Docket No. 216780US-2 DIV

IN RE APPLICATION OF: SATOSHI SHIMIZU ET AL

SERIAL NO: 10/028,766

FILED: DECEMBER 28, 2001

FOR: MIS TRANSISTOR AND METHOD OF FABRICATING THE SAME

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

Transmitted herewith is an amendment in the above-identified application.

- ■ No additional fee is required
- □ Small entity status of this application under 37 C.F.R. §1.9 and §1.27 is claimed.
- ■ Additional documents filed herewith: Marked-Up Copy of Amendment

The Fee has been calculated as shown below:

CLAIMS	CLAIMS REMAINING		HIGHEST NUMBER PREVIOUSLY PAID	NO. EXTRA CLAIMS	RATE	CALCULATIONS
TOTAL	4	MINUS	20	0	× $18 =	$0.00
INDEPENDENT	2	MINUS	3	0	× $84 =	$0.00
		□ MULTIPLE DEPENDENT CLAIMS			+ $280 =	$0.00
		TOTAL OF ABOVE CALCULATIONS				$0.00
		□ Reduction by 50% for filing by Small Entity				$0.00
		□ Recordation of Assignment			+ $40 =	$0.00
		TOTAL				$0.00

- □ A check in the amount of is attached.
- ■ Please charge any additional Fees for the papers being filed herewith and for which no check is enclosed herewith, or credit any overpayment to deposit Account No. 15-0030. A duplicate copy of this sheet is enclosed.
- ■ If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time may be charged to Deposit Account No. 15-0030. A duplicate copy of this sheet is enclosed.

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216780US-2 DIV

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF:

SATOSHI SHIMIZU ET AL. : GROUP ART UNIT: 2811

SERIAL NO: 10/028,766

FILED: DECEMBER 28, 2001 : EXAMINER: NGUYEN, C.

FOR: MIS TRANSISTOR AND METHOD OF FABRICATING THE SAME

AMENDMENT

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

In response to the Office Action of July 25, 2002, please amend the above-identified application as follows:

IN THE CLAIMS

Please amend Claims 10 and 12 to read as follows:[1]

10. (Amended) A MIS transistor including:

a gate electrode being formed to be opposed to a silicon substrate through a gate insulating film;

side walls being formed on said silicon substrate on both sides of said gate electrode, said side walls being higher than said gate electrode; and

[1]A marked-up copy of the amendments is attached hereto.